ConScience

Quantum Pilot Line - MPW Program: Technical & Operational Guide for participants

version 1.0 — February 2026
Author: Lert Chayanun, Ph.D. (Q-MPW program coordinator)

1. Introduction

The ConScience Quantum Pilot line - Multi-Project Wafer (MPW) Program enables researchers, and startups to fabricate superconducting quantum circuits using a shared wafer run. This guide provides all technical and procedural information required to prepare designs, submit layout files, understand the fabrication workflow, and receive finished chips.

The document is intended for designers participating in an MPW round. It outlines:

- the MPW wafer structure and design constraints
- the complete set of layer convention and design rules
- submission requirements and file formats
- Design check and feedback process
- wafer layout assembly
- fabrication and post-fabrication workflows

The MPW program operates on a **quarterly fabrication cycle**, with each round following a fixed submission, review, and production timeline. Because the MPW program involves proprietary circuit designs and controlled superconducting technology, participation is conducted under a confidentiality framework (Section 3) and subject to applicable export-control regulations (Section 10). These requirements are described in dedicated sections later in the document and apply to all participants.

By following the guidelines in this document, participants can ensure that their designs are compatible with the Foundry process and that submissions proceed smoothly through review, fabrication, and delivery.

2. MPW Program Overview

ConScience Quantum Foundry Multi-Project Wafer (Q-MPW) Program provides shared access to a superconducting fabrication process, enabling multiple participants to integrate their designs onto a single wafer. Each MPW round is part of a **recurring quarterly cycle**, ensuring predictable planning for participants and consistent wafer availability throughout the year. This section describes the wafer structure, design boundaries, and key process characteristics that customers should understand before preparing their layouts.

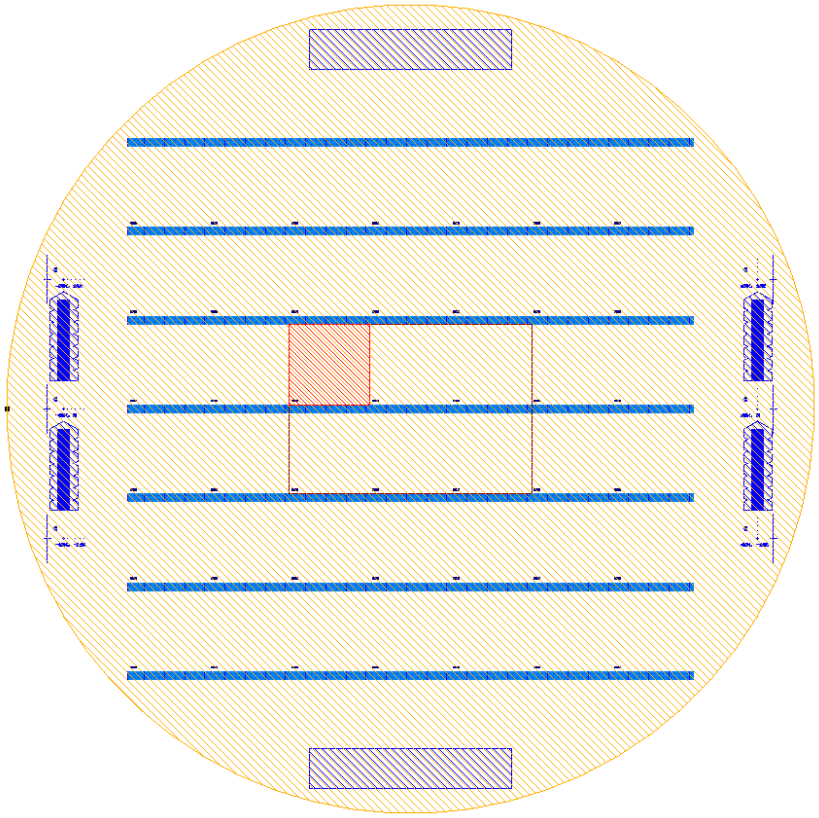
© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

2.1 Wafer and Block Structure

Each MPW run uses a standardized wafer layout designed to accommodate multiple independent designs while maintaining predictable fabrication performance.

- The wafer is divided into **20 × 30 mm Blocks**.
- Each Block contains **six 10 × 10 mm chip slots**.
- Participants receive a **predefined number of Blocks** based on the MPW tier they enroll in; **tier and pricing information is available upon request**.
- A single design may be placed in one or multiple chip slots, depending on customer preference and available capacity.

This structure ensures predictable placement, efficient wafer utilization, and consistent electrical performance across all designs.



Figur 1 Q-MPW wafer layout overview with ConSciece's infrastructure, including alignment marks, process monitoring, and JJ test structures. A basis block of 20 × 30 mm is highlighted with a brown rectangular and 10 × 10 mm chip is a red rectangular.

2.2 Design Capacity and Limits

To maintain schedule reliability and ensure high-quality fabrication, each MPW round supports:

- Up to **2 distinct chip designs for each participant**
- A maximum design size of **10 × 10 mm** per chip slot
- One design per GDS file (see Section 5)

Designs must comply with all rules in Section 4 to be eligible for integration into the wafer.

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

2.3 Process Technology Overview

All MPW runs use ConScience's qualified superconducting process, which includes:

- 300 nm aluminum ground plane on a high-resistivity silicon wafer (500 µm thick)
- Manhattan-style Josephson junctions
- Airbridge structures

This process is optimized for superconducting quantum circuits such as:

- Transmon qubits with coherence times T_1 up to 250 µs
- Coplanar waveguide (CPW) resonators with internal quality factor up to 1 million

2.4 Expected Process Variation

As with all superconducting fabrication processes, some variation is inherent. Participants should design with the following typical values in mind:

- **Global Josephson junction resistance variation:** ±20%
- **Local variation within a Block:** ±10%

These values represent the expected process window for MPW runs and should be considered when designing qubits, resonators, and other sensitive components.

2.5 What Customers Receive

Participants in an MPW round receive:

- A placement map showing where their designs appear on the wafer
- Fabricated chips corresponding to their purchased Blocks
- Data of Josephson junction resistance variation
- A delivery report summarizing fabrication and dicing outcomes

This ensures full transparency from submission through delivery.

3. Confidentiality and NDA Requirements

Participation in the Q-MPW Program involves the exchange of proprietary design data and Foundry process information. To ensure a secure and trusted shared-wafer environment, all participants must enter into a Non-Disclosure Agreement (NDA) with ConScience before submitting any design files.

The NDA defines how design data and communication are handled throughout the MPW round. To protect the intellectual property and proprietary research of all participants:

- Each participant's design files, layout geometry, and technical details are treated as strictly confidential.
- No participant will have access to, visibility of, or information about any other participant's design, including geometry, placement, Block allocation, or submission metadata.
- Only the submitting participant and the Foundry have access to a given design during review, wafer integration, fabrication, and delivery.
- Wafer-level previews shared during the process include only the participant's own chip(s) and Foundry-added identifiers.

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

- Internal Foundry workflows ensure that design data is compartmentalized and handled on a need-to-know basis by authorized personnel only.

These confidentiality protections apply across all stages of the MPW workflow, including design review, wafer assembly, fabrication, export, and post-fabrication reporting.

4. Layer Convention and Design Rules

This section defines the layer usage, geometric constraints, and structural requirements for all designs submitted to the ConScience Quantum Foundry MPW program. Customers must adhere to the layer convention and design rules described below to ensure manufacturability, process compatibility, and predictable device performance.

4.1 Layer Convention

The MPW program uses a fixed layer convention. Customers must use only the layers listed below and follow the naming and numbering scheme exactly.

Layer Name (Variable)	Layer Number / Datatype	Description / Purpose
wafer_marks	10 / 0	Global wafer-level alignment marks
chip_marks	20 / 0	Chip-level alignment marks
top_chip_marks	30 / 0	Top-side chip alignment marks
bottom_chip_marks	40 / 0	Bottom-side chip alignment marks
dicing_marks	50 / 0	Dicing/sawing alignment marks
frontend_100	100 / 0	Reserved frontend placeholder (empty / Beamer output)
gnd_patterning	110 / 0	GND patterning placeholder (empty / Beamer output)
gnd_etch	111 / 0	Main GND metal etching layer
gnd_mask	112 / 0	GND masking layer
gnd_flux_holes	113 / 0	Flux-hole openings in GND metal
gnd_flux_mask	114 / 0	Mask for flux-hole patterning
gnd_marks	119 / 0	GND-level alignment marks
jj_man_base	120 / 0	JJ Manhattan base (empty / Beamer output)
jj_man_h	121 / 0	JJ Manhattan horizontal arm
jj_man_v	122 / 0	JJ Manhattan vertical arm
jj_man_tips	123 / 0	JJ Manhattan tips
jj_man_marks	129 / 0	JJ Manhattan placement markers (10 µm squares)

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

at_feet_base	170 / 0	Airbridge feet base (empty / Beamer output)
at_feet_open	171 / 0	Airbridge feet openings
at_feet_marks	179 / 0	Airbridge feet alignment marks
at_arch_base	180 / 0	Airbridge arch base (empty / Beamer output)
at_arch_open	181 / 0	Airbridge arch openings
at_arch_marks	189 / 0	Airbridge arch alignment marks
wafer_support	1110 / 0	Wafer-level support structures
chip_support	1120 / 0	Chip-level support structures
text_area	1130 / 0	Text annotation area
bump_area	1140 / 0	Bump-bonding keep-out or placement area
fc_mark_area	1150 / 0	Flip-chip mark area

Marker Layers (900–999 Range)

These are generated by DRC rules, not drawn in the layout.

Marker Layer	Rule ID	Meaning
911 / 0	1.1	GND Etch — Minimum Linewidth
912 / 0	1.2	GND Etch — Minimum Spacing
921 / 0	2.1	Airbridge Feet — Minimum Size
922 / 0	2.2	Airbridge Feet — No Overlap with Metal
923 / 0	2.3	Airbridge Feet — Minimum Clearance
924 / 0	2.4	Airbridge Arch — Feet Overlap
925 / 0	2.5	Airbridge Span — Max 75 µm
931 / 0	3.1	Flux Holes — Forbidden in Waveguide
932 / 0	3.2	Flux Holes — Too Close to Metal
933 / 0	3.3	Flux Holes — In Isolated Metal Regions

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

4.2 Chip Area Constraint

Rule Group	Rule ID	Rule Name	What the Rule Verifies	Layers Checked
0. Chip Boundary	**0.1**	Chip Size Limit (±5000 µm)	Ensures all key layers stay within the allowed chip outline.	171, 181, 111, 113
1. GND Etch Rules	**1.1**	Minimum Linewidth	GND etch features must be ≥ 3 µm wide.	111
	1.2	Minimum Spacing	Spacing between GND etch features must be ≥ 3 µm.	111
2. Airbridge Rules	**2.1**	Feet Minimum Size	Airbridge feet openings must be ≥ 10 µm.	171
	2.2	Feet Non-Overlap with Metal gap	Airbridge feet must not overlap etched GND metal.	171, 111
	2.3	Feet Clearance	Airbridge feet must maintain ≥ 2 µm clearance from GND metal.	171, 111
	2.4	Arch–Feet Overlap	Airbridge arches must properly overlap their feet.	171, 181
	2.5	Arch Span Limit	Arch span must be ≤ 75 µm; also checks malformed arches.	181, 171
3. Flux Hole Rules	**3.1**	No Flux Holes in Waveguide	Flux holes must not appear inside CPW waveguide regions.	113, derived CPW from 111
	3.2	Flux Holes Too Close to Metal	Flux holes must not touch or be within 10 µm of CPW.	113, 111
	3.3	Flux Holes in Isolated Metal	Flux holes must not appear inside isolated metal islands.	113, 111
4. JJ Manhattan Rules	**4.1**	JJ Placeholder Size	JJ Manhattan marks must be 10 µm × 10 µm.	129
	4.2	JJ Containment	JJ marks must be fully inside GND etch.	129, 111
	4.3	JJ Placement Geometry	JJ marks must be 5 µm from top/right metal edges and not 5 µm from left/bottom.	129, 111

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

5. Submission Guidelines

This section describes how participants must prepare and deliver their design files for inclusion in the MPW round. Following these guidelines ensures a smooth review process and minimizes delays during wafer assembly.

5.1 Preparing a GDS File

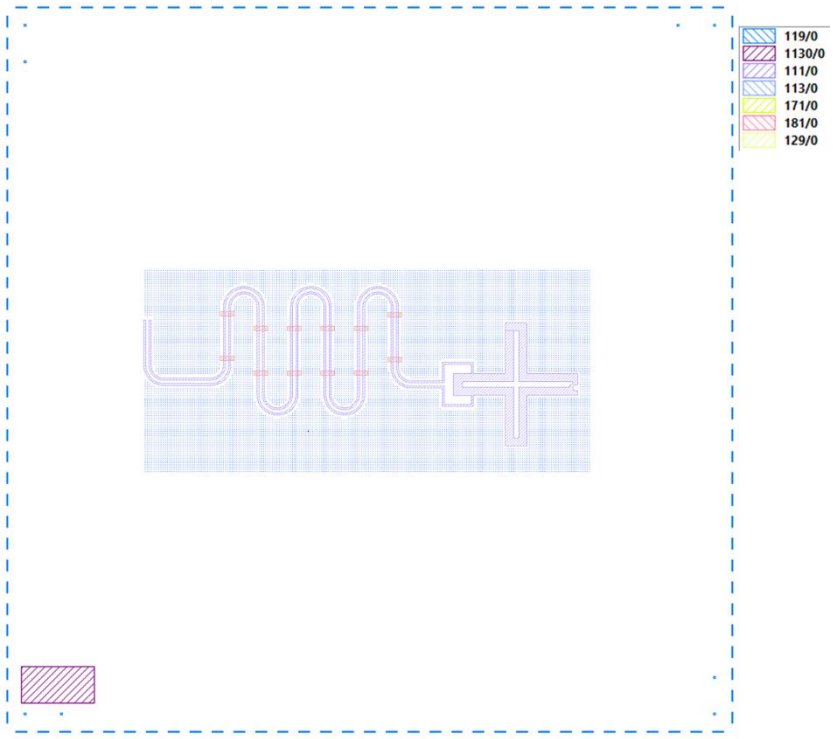
All submissions should be in **GDSII format**. When creating your layout, designers are expected to adhere to these guidelines:

Q-MPW Template

Participants are required to use the official **ConScience_QMPW_Template**, which features:

- A **dicing street / maximum chip outline** (layer 119) marking the standard chip boundary (10 mm × 10 mm)
- An **exclusion zone** (layer 1130) designated for identifiers added by the Foundry
- **Local alignment structures** (layer 119)
- **JJ placeholder cell** (layer 129) - use to mark JJ locations as per rule 4, section 3.2.
- The origin point (0,0) positioned at the **center** of the design

The template offers reference geometry and infrastructure patterns but does **not** limit your design area to less than the maximum allowed size of 10 × 10 mm. If your chip is smaller than this maximum, you must define your own chip boundaries, matching the structure given in the template. Additionally, even with a smaller chip, you must retain the provided 10 × 10 mm boundaries from the template, as these are necessary for wafer layout assembly.



Figur 2 ConScience_QMPW_Template overview, containing a chip outline and chip marks in layer 119, and an exclusion zone in layer 1130. The example of qubit design with layers mentioned in section 3.1 is also included at the center (not to scale).

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

5.2 Alignment Integration

Participants do not need to take any action regarding alignment. All alignment is performed using **global wafer marks** and, if present, **local alignment structures included in the MPW template**.

Participants must not modify or obscure any template-provided alignment structures.

5.3 Multiple Designs and File Naming

Participants may submit up to **two distinct chip designs** per MPW round. Starter-tier participants (single-Block allocation) are encouraged to submit **one primary design**, as redundancy within a single Block is limited.

Required Naming Convention

Each GDS file must follow this format:

ParticipantName_DesignName_vX.Y.gds

Examples:

- QubitLab_ResonatorTest_v1.0.gds
- QuantumStart_Q1Array_v2.3.gds

Each design must be submitted as a **separate GDS file**.

5.4 Version Control Requirements

To maintain clarity during review and fabrication:

- Submit **only one final version** of each design
- Increment version numbers for any resubmission
- Ensure the README and design list match the final versions
- Do not submit multiple versions unless explicitly requested

The Foundry will fabricate only the version marked as **final**.

5.5 Submission Method

Email Submission (Primary Method)

Participants should send their submission package via email to the MPW coordination team.

Guidelines:

- Compress all files into a single ZIP archive
- Include the README and design list see Appendix A for README template
- Refer to Appendix B for submission checklist
- Use the subject line: **“MPW Submission — [Participant Name] — [Round ID]”**

5.6 Deadlines

The MPW program follows a **quarterly schedule**. Participants can find the current timeline:

- On the MPW program webpage

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

- In the round announcement email

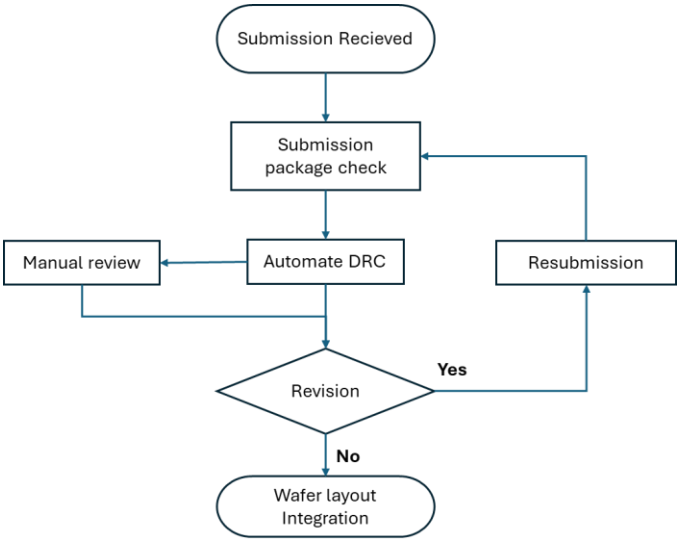
To support smooth wafer assembly:

- Submit all files before the published deadline
- Late submissions may be deferred to the next round

The Foundry will communicate any schedule changes as early as possible.

6. Design Review Workflow

After receiving a submission, the Foundry performs a structured review to ensure the design is manufacturable and compliant with MPW rules.



Figur 3 Design review workflow overview

6.1 File Intake

The Foundry verifies that the GDS file opens correctly, follows the required naming convention, matches the version listed in the README, and fits within the MPW template. Any blocking issues are communicated immediately.

6.2 Design Rule Check

The design is evaluated using automated and manual checks. Automated checks confirm compliance with minimum feature sizes, spacing rules, airbridge constraints, and JJ placeholder clearance. Manual inspection covers waveguide continuity, and template integrity.

6.3 Feedback and Revision

If any issues are identified, the participant will receive a detailed report outlining the violations in accordance with the rules specified in section 3.2. The participant has the opportunity to revise and resubmit their materials. The Foundry will verify the corrections prior to proceeding. Participants are expected to respond promptly to any feedback from the DRC.

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

6.4 Acceptance

A design is accepted once all rules are satisfied and the final version is confirmed. Accepted designs move to wafer integration.

7. Wafer Integration Workflow

After acceptance, the design is incorporated into the MPW wafer. This process is handled internally to protect participant confidentiality.

7.1 Chip Placement

Each design is placed into the wafer layout according to the participant's Block allocation and duplication preferences. Placement of other participants' designs is not disclosed.

7.2 Infrastructure Integration

The Foundry adds the wafer run ID, chip identifier, exclusion-zone markings, and any template-defined alignment structures. These additions do not modify customer geometry.

7.3 Customer Preview

Participants receive a preview of **only their own chip(s)**, showing the chip boundary, exclusion zone, and Foundry-added identifiers. The full wafer layout is not shared. Once the participant confirms the preview, the layout is locked for fabrication.

8. Fabrication Workflow

The MPW wafer proceeds through the standard superconducting fabrication sequence, including Aluminium ground plane deposition, patterning, Josephson junction formation, and airbridge fabrication. Expected process variation follows the values listed in Section 2.4. Foundry test structures are included for process monitoring, and data may be shared upon request.

9. Post-Fabrication Workflow

After fabrication, the wafer is diced into chips. Participants receive chips coated with a removable protective photoresist. The photoresist can be dissolved in acetone at room temperature for 10 minutes, then rinsed with IPA and dried with N2—***Do not use a sonicator!, as ultrasound can damage airbridges***. Each delivery includes a report detailing chip identifiers, dicing notes, and available test data.

10. Export Procedure

The device fabricated from this program is classified as **dual-use** under **Annex 1, Category 3: Electronics (3A001)**. It falls under the following definition:

Electronic devices and circuits containing components manufactured from *superconductive* materials, specially designed for operation below the *critical temperature* of at least one superconductive constituent, and meeting any of the following criteria:

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

1. Current switching for digital circuits using superconductive gates with a delay-time–power-dissipation product < 10^{-14} J;
2. Frequency selection at any frequency using resonant circuits with Q-values > 10 000.

Such items may be used for both civilian and military applications.

10.1 End-User Statement (EUS) Requirement

To comply with EU dual-use regulations and internal export-control procedures, **all participants must submit an End-User Statement (EUS) before shipment of fabricated devices, regardless of destination.**

The EUS confirms:

- the identity of the end user,
- the intended use of the devices,
- that the devices will not be diverted to prohibited applications or destinations.

Shipment cannot be initiated until a complete and signed EUS has been received and verified. See Appendix D for ConScience's EUS template.

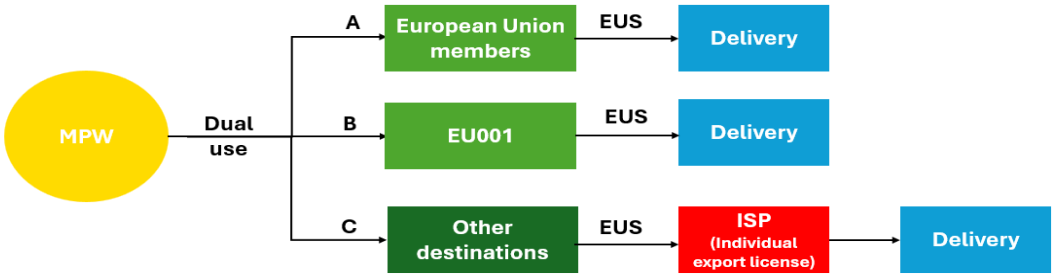


Figure 4 Export-process flow for MPW shipments, distinguishing between intra-EU transfers, EU001-authorised destinations, and destinations requiring an individual export licence.

10.2 Export Control Destination Categories

A. Transfers within the **European Union members** are treated as intra-EU movements and generally do not require an individual export license. This applies to shipments from Sweden to any EU Member State (Austria, Belgium, Bulgaria, Croatia, Cyprus, Czechia, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Poland, Portugal, Romania, Slovakia, Slovenia, Spain, Sweden).

B. For exports to destinations covered by the EU General Export Authorisation **EU001**, dual-use items listed in Annex I—including 3A001 superconducting electronics—may be shipped without an individual export license. EU001 destinations include; Australia, Canada, Iceland, Japan, Liechtenstein, New Zealand, Norway, Switzerland, United Kingdom, United States.

C. Shipments to all **other destinations** require an **individual export license**, and delivery schedules will depend on the license-approval timeline. As shown in (Figure 4), export-control processing can introduce substantial lead times beyond fabrication and courier transit. To help ensure that deliveries

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

align with the planned end-of-quarter shipment, participants are strongly encouraged to begin export-control discussions early in the MPW round. Early preparation of end-user documentation and any required licensing information significantly reduces the risk of delays once fabrication is complete.

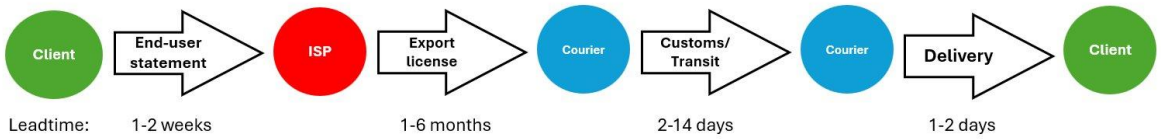


Figure 5 Overview of the export process from end-user statement to final delivery. The diagram highlights the additional export-license stage required for destinations outside the EU and EU001 group and the corresponding impact on total delivery time.

End-User Statement Requirement

To comply with EU dual-use regulations and internal export-control procedures, **all participants must submit an End-User Statement (EUS)** before shipment of fabricated devices—**regardless of destination**.

The EUS confirms:

- the identity of the end user,
- the intended use of the devices,
- that the devices will not be diverted to prohibited applications or destinations.

Shipment cannot be initiated until a complete and signed EUS has been received and verified. See **Appendix D** for ConScience's EUS template.

11. Appendices

Appendix A — README Template (Example for Participants)

```
# MPW Submission README

Participant: [Your Name / Organization]
MPW Round: [Round ID]
Submission Date: [YYYY-MM-DD]

## Submitted Designs
1. Design Name: [Name]
  File: [Participant_Design_vX.Y.gds]
  Version: vX.Y
  Notes: [Optional]

2. Design Name: [Name]
  File: [Participant_Design_vX.Y.gds]
  Version: vX.Y
```


© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

Notes: [Optional]

Duplication Preferences
- [Design 1]: [Number of copies per Block]
- [Design 2]: [Number of copies per Block]

Contact Information
Primary Contact: [Name]
Email: [Email]
Phone (optional): [Phone]

Additional Notes
[Optional: Any clarifications, special requests, or comments]

Appendix B — Submission Checklist (For Both Customer and Foundry)

This checklist ensures that nothing is missed during submission and intake.

1. GDS Preparation

- [ ] Used the official MPW template
- [ ] Design fits within 10 × 10 mm
- [ ] No geometry in the exclusion zone
- [ ] Coordinate origin at (0,0) center
- [ ] Only approved MPW layers used
- [ ] No unintended shapes on unused layers

2. File Naming & Structure

- [ ] One design per GDS file
- [ ] Correct naming convention used
- [ ] Final version only (vX.Y)
- [ ] No extra or outdated versions included

3. Documentation

- [ ] README completed using the template
- [ ] Design list included (or embedded in README)
- [ ] Duplication preferences clearly stated
- [ ] Contact information provided

4. Packaging

- [ ] All files placed in a single ZIP archive

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.

- [ ] ZIP archive named appropriately
- [ ] Email subject line formatted correctly

5. Submission

- [ ] Sent to MPW coordination email
- [ ] Sent before the deadline
- [ ] Awaiting confirmation of receipt

Appendix C — KLayout Template

(Description + link)

Appendix D — End-User Statement

(Description + link)

Appendix E — FAQ

Common questions from academics and startups.

© ConScience 2026. All rights reserved.
Images may not be used, reproduced, or distributed without prior written permission.